UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,658	07/19/2001	Chandrasekhar Thyamagondlu Srinivasaiah	CISCO-4330	1822

7590 02/17/2004

David B. Ritchie
Thelen Reid & Priest LLP
P. O. Box 640640
San Jose, CA 95164

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/909,658	Applicant(s) SRINIVASAIAH ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1 to 26** are presented for examination.

Drawings

2. a) The **drawings** are objected to because of the problems addressed in the attached PTO-948. Correction is required.

b) Figures 1 and 2 should be designated by a **legend such as --Prior Art--**. See MPEP § 608.02(g).

Claim objections

3. Claims 5, 12, and 19, are objected to because of the following informalities:

(a) Please change the term "the inverted phase" to --an inverted phase-- on line 2 of claim 5.

(b) Please change the term "the inverted phase" to --an inverted phase-- on line 2 of claim 12.

(b) Please change the term "the inverted phase" to --an inverted phase-- on line 2 of claim 19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims **1-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Wu et al. (U.S. PN: 6,286,119) in view of Miller (6,606,575).

As per claims **1, 8 and 15,** Wu et al. in figure 2 disclose or teach two interconnected IC chips, sending IC chip (211) and receiving IC chip (213) interconnected on a board implemented for delay fault test and further each of the IC chips includes a TAP controller (215) including an IEEE 1149.1 standard TAP controller for performing IEEE 1149.1 standard TAP operations and an associated modifier for modifying standard TAP signals. Wu et al. teach that the interconnect delay test uses the IEEE 1149.1 standard allows board and system designers to add new AC interconnect tests for any signals at any time (see abstract) and further Wu et al. teach that data stored in boundary scan cells included in the first IC chip is transferred to the second IC chip via the interconnect between the first and second IC chips and the transferred data is captured by the second chip (see col. 2, lines 58-64). Wu et al. in figure 3, shows under normal IEEE 1149.1 standard operation, each of the boundary scan cells updated upon the rising edge of the load signal and captures at the rising edge of the scan test clock control signal is 0 (see col. 5, lines 25-34). Furthermore, Wu et al. teach that signals commonly synchronized at the corresponding system clock edges whereby data is launched at a rising edge of a system clock and the data usually sampled by receivers at the rising edge of its next system clock cycle (see col. 9, lines 10-35). Although, Wu et al. teach phase operations associated to the test data or test vectors Wu et al. **do not explicitly** teach comparing the reference (source) data with the test data. **However,**

Miller teach calibrating timing of test signals of an integrated circuit wherein a test signal compared by a compare circuit (XOR) to a reference signal and a delay of each channel adjusted to maximize cross-correlation between the test signal and the reference signal (see abstract and figures 6-9). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to combine (incorporate) the teachings of Wu et al. to include a comparator to compare reference signals with test signals as taught by Miller to produce data value to an amount of phase correlation between the reference and data signals (see col. 3, lines 65-67). **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to employ a process for adjusting the test signal calibration delays of an IC tester channels so that the test signal timing be closely coordinated (see col. 3, lines 40-48).

As per claims **2, 3, 9, 10, 16, and 17,** Wu et al. in view of Miller teach all the subject matter claimed in claims 1, 8 and 15 including Wu et al. in figure 6 disclose a reset signal (RST) is fed to the reset terminals R of two D-FFs (323 and 325) (see col. 7, lines 45-50). Further, Miller in figure 5 teaches that after programming control and timing circuit (46) and reference signal generator (58) to produce TEST and REF signal having the same pattern, a host computer resets (zero value) the counter (68) (see col. 8, last paragraph).

As per claims **4-6, 11-13 and 18-20,** Wu et al. in view of Miller teach all the subject matter claimed in claims 1, 8 and 15 including Miller in figure 6 teaches a block diagram of an apparatus includes a compare circuit (60) for comparing the TEST and REF signals and producing an output MATCH signal which the MATCH output of compare circuit (60) indicates how the amplitude of the TEST signal matches that of the REF signal. Wu et al. in view of

Miller **do not explicitly teach** inverting the phase if the output does not match. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, the methods of inverting phases or bits are required when the computing signals do not match. **Accordingly,** it would have been obvious to one ordinary skill in the art to include an inverter because such logic gate would have been required in order to match the un-matched signals or phases.

As per claims 7, **14 and 21,** Wu et al. in view of Miller teach all the subject matter claimed in claims 1, 8 and 15 including Miller in figure 6 teach a register (66) for storing the output after the test signal and reference signals compared.

As per claims **22-26,** Wu et al. in view of Miller teach all the subject matter claimed in claims 1, 8 and 15 including Wu et al. in figure 2 disclose or teach two interconnected IC chips, a sending IC chip (211) and a receiving IC chip (213) interconnected on a board implemented for delay fault test and further each of the IC chips includes a TAP controller (215) including an IEEE 1149.1 standard TAP controller for performing IEEE 1149.1 standard TAP operations, an associated modifier for modifying standard TAP signals, boundary scan cells (BSC) (217) which the BSC according to the IEEE 1149.1 standard and further the IEEE 1149.1 standard allows board and system designers to add new AC interconnect tests for any signals at any time (see abstract). Further, Miller teach calibrating timing of test signals of an integrated circuit wherein the test signal compared by a compare circuit (XOR) to a reference signal and the delay of each channel is adjusted to maximize cross-correlation between the test signal and the reference signal (see abstract and figures 6-9). Wu et al. in view of Miller **do not teach or show** boundary scan cells (BSC) comprising first and second flip-flops connected to a multiplexer. **However,** Wu et

al. in figure 2 teach an IEEE 1149.1 standard TAP controller for performing IEEE 1149.1 standard TAP operations (215), an associated modifier for modifying standard TAP signals and boundary scan cells (BSC) (217) which the BSC according to the IEEE 1149.1 standard commonly include first and second flip-flops connected to a multiplexer. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include all the claimed components of BSC such as first and second flip-flops connected to a multiplexer with in the Wu et al's boundary scan cells since the components are known to the IEEE 1149.1 standard. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because claimed components are well known futures of boundary scan cells according to the IEEE 1149.1 standard.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,444,715 Gruetzner et al.

US PN: 6,199,182 Whetsel

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner